Notice of Allowability	Application No.	Applicant(s)	
	10/642,519	KUWATA ET AL.	
	Examiner	Art Unit	
	JAISON JOSEPH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 8/20/2009*.

2. ☒ The allowed claim(s) is/are *9, 10 and 8 renumbered as 1 - 3 respectively*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Thomas E. McKiernan on 8/27/2009.

The application has been amended as follows:

Claim 10 rewrite as: A discrimination circuit for a data signal having duty cycle deviation for use in an optical receiver, comprising:

a phase locked loop (PLL) circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec);

a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point at which said PLL circuit is locked; and

a control circuit for controlling, based on a result of said evaluation, a data discrimination phase before and after the point at which said PLL circuit is locked, wherein:

said PLL circuit discriminates said input data every other bit by using said clock signal whose frequency is equal to one half the data transmission rate and an inverted version of said clock signal, and achieves a phase lock in accordance with a result obtained by **a first** exclusive-ORing the data discriminated by a clock signal delayed in phase by one half cycle of said data signal with the data discriminated by said half-frequency clock signal and the data discriminated by the inverted version of said half-frequency clock signal, respectively, and by comparing average values **of sums** of said respective **first** exclusive-OR ~~sums~~,

said duty cycle evaluation circuit evaluates said duty cycle to determine whether said duty cycle changes from "narrow" to "wide" or from "wide" to "narrow" between said input data before and after the point at which said PLL circuit is locked, said evaluation being made based on a result obtained by **a second** exclusive-ORing the data discriminated by an inverted version of said clock signal delayed in phase by one half cycle of said data signal with the data discriminated by said half-frequency clock signal and the inverted version of said half-frequency clock signal, respectively, and by comparing average values **of sums** of said respective **second** exclusive-OR ~~sums~~, and

said control circuit, based on the result of said evaluation, controls the phase of said clock signal delayed in phase by one half cycle of said data signal and the phase of the inverted version of said clock signal respectively in opposite directions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: claims 9, 10 and 8 are allowable over prior art of record. The prior art of record failed to teach a discrimination circuit for a data signal having duty cycle deviation for use in an optical receiver, comprising: a phase locked loop (PLL) circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec); a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point at which said PLL circuit is locked; and a control circuit for controlling, based on a result of said evaluation, a data discrimination phase before and after the point at which said PLL circuit is locked, wherein: said control circuit includes an initial phase setting circuit in which duty cycle information representing an initial phase adjustment is set; and said initial phase setting circuit compares said duty cycle information representing said initial phase adjustment with an output of said duty cycle evaluation circuit and, when locked in phase in the same condition as said duty cycle information representing said initial phase adjustment, said locked condition is maintained, but when locked in phase in a condition different from said duty cycle information representing said initial phase adjustment, a clock output of a voltage-controlled oscillator in said PLL circuit is inverted as claimed in independent claim 9 and similarly claimed in independent claim 10. Therefore claims 8 - 10 are novel and non-obvious over prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAISON JOSEPH whose telephone number is (571)272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. J./
Examiner, Art Unit 2611

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611